CLEAN VERSION OF AMENDED SPECIFICATION PARAGRAPHS

ELECTRONIC ASSEMBLY WITH FILLED NO-FLOW UNDERFILL AND METHODS OF MANUFACTURE

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The sub-title on page 1, line 7.Technical Field .

The paragraph beginning on page 1, line 9.

The present subject matter relates generally to electronics packaging. More particularly, the present subject matter relates to an electronic assembly that includes a component package, such as an integrated circuit (IC) package, comprising a filled no-flow underfill material to increase yield and reliability, and to manufacturing methods related thereto.

The sub-title on page 1, line 15. Background Information

The paragraph beginning on page 4, line 12.

In the following detailed description of embodiments of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice them , and it is to be understood that other embodiments may be utilized and that structural, mechanical, compositional, procedural, and electrical changes may be made without departing from the spirit and scope of the present subject matter.. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of embodiments of the present invention is defined only by the appended claims.

The paragraph beginning on page 4, line 22.

Embodiments of the present invention provide a solution to various yield and reliability problems that are associated with prior art no-flow underfills for high performance component packages, such as IC packages, by employing a filled no-flow underfill, and by utilizing pressure

to force the component bumps against the package pads to displace substantially all particles from between the component bumps and the package pads to provide good electrical contact. Various embodiments are illustrated and described herein.

The paragraph beginning on page 5, line 24.

FIG. 1 is a block diagram of an electronic system incorporating at least one electronic assembly comprising a component package with a filled no-flow underfill, in accordance with one embodiment of the invention. Electronic system 1 is merely one example of an electronic system in which the present subject matter can be used. In this example, electronic system 1 comprises a data processing system that includes a system bus 2 to couple the various components of the system. System bus 2 provides communications links among the various components of the electronic system 1 and can be implemented as a single bus, as a combination of busses, or in any other suitable manner.

The paragraph beginning on page 8, line 24.

Underfill 116 includes a filler having a plurality of particles 120.. In one embodiment, the filler comprises an agent to reduce the CTE (coefficient of thermal expansion). The filler is selected from the group comprising silica, silicon oxide, silicon dioxide, silicon nitride, aluminum oxide, and aluminum nitride. The filler can also be selected from the group comprising any ceramic oxide and any ceramic nitride.

The paragraph beginning on page 9, line 12.

The filler particles 120 can have a size in the range of 0.05 microns to 40 microns.

The paragraph beginning on page 9, line 14.

In one embodiment, particles 120 are substantially spherical, while in other embodiments

particles 120 are not spherical and are thus generally less expensive when purchased from suppliers.

The paragraph beginning on page 10, line 27.

Concurrently, or subsequently, suitable pressure is applied to component 130, to package substrate 110, or to both component 130 and package substrate 110, to cause bumps 132 to squeeze out any particles 122 that would otherwise be interposed between bumps 132 and pads 112, so that particles 122 do not remain between bumps 132 and pads 112. For example, particles 122 are shown being squeezed away from the joint between bumps 132 and pads 112 in the directions indicated by arrows 123.

The paragraph beginning on page 11, line 4.

It may not be essential to squeeze out every particle 122, depending upon the size and shape of particles 122. It is possible that one or more particles 122 may become embedded in one of bumps 132 and/or its corresponding pad 112 without unduly preventing adequate physical and electrical contact after solder join. However, suitable pressure is applied to cause bumps 132 to physically contact pads 112, so that during a subsequent solder reflow operation bumps 132 and pads 112 will be in adequate electrical contact.

The paragraph beginning on page 11, line 11.

Although in FIG. 6, pads 112 are illustrated as partially melted and as having slightly distorted upper portions that are being attracted to corresponding bumps 132 through surface tension forces, it will be understood, as described elsewhere herein, that heat need not necessarily be applied concurrently with pressure.

The paragraph beginning on page 14, line 17.

The above-described choice of materials; geometry; sequence of operations; equipment for applying pressure; equipment for applying heat; and part dimensions can all be varied by one

of ordinary skill in the art to optimize fabrication of component packages in accordance with the present subject matter.

The paragraph beginning on page 14, line 21.

Various embodiments of component packages, including IC packages, electronic assemblies, and electronic systems, including computer systems, can be implemented using various types of components, package substrates, underfill materials, various types of fabrication equipment, and various fabrication sequences, to achieve the advantages of the present disclosure.

The paragraph beginning on page 14, line 26.

FIGS. 1-7 are merely representational and are not drawn to scale. Certain proportions thereof may be exaggerated, while others may be minimized. FIGS. 5-8B are intended to illustrate various implementations of the disclosure that can be understood and appropriately carried out by those of ordinary skill in the art.

The paragraph beginning on page 15, line 3.

The present subject matter provides for methods of fabricating high-yield, high reliability, component packages, such as flip-chip IC packages, having filled, no-flow underfill. Pressure is applied via a suitable tool, such as a thermocompression bonder, ultrasonic bonder, chip placement tool, instant chip join tool, or the like, to force corresponding terminals of the component and package substrate into close physical contact, and to displace substantially all filler particles from between the component terminals and the substrate terminals to provide good electrical and mechanical contact.

The paragraph beginning on page 15, line 24.

Application of various methods to a component package, an electronic assembly, and an electronic system are also described. An electronic system and/or data processing system that incorporates one or more electronic assemblies that utilize the present subject matter can be fabricated in less time and at less cost, while maintaining high yield and high reliability, and such systems are therefore more commercially attractive.

The paragraph beginning on page 16, line 8.

Embodiments of the present invention are not to be construed as limited to use in ball-grid array packages, C4 (controlled collapse component connect), or any other type of component packages, and they can be used with any type of component package where the herein-described features of the present subject matter provide an advantage.

The paragraph beginning on page 16, line 12.

While the subject matter has been illustrated and described with regard to ICs mounted upon IC substrates, embodiments of the invention are not to be limited to such applications, and they can also be used for other types of electronic packages and other types of components, such as passive components, hybrid modules, printed circuit boards, mezzanine boards, and for any other type of electrical structure requiring underfill.

The paragraph beginning on page 16, line 17.

While the embodiment shown in FIGS. 5-7 has been described with reference to a single component, embodiments of the invention are not limited to packaging single components and can be used for packaging multiple components, e.g. multi-chip IC packages or multi-chip modules.

The paragraph beginning on page 16, line 21.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present subject matter. Therefore, it is manifestly intended that embodiments of this invention be limited only by the claims and the equivalents thereof.